

NL
PH031056

MAT.

DOSSIER
Europäisches Patentamt

(19)



European Patent Office

Office européen des brevets



(11)

EP 0 851 605 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
01.07.1998 Bulletin 1998/27(51) Int. Cl.⁶: H04B 7/08, H04B 1/16

(21) Application number: 97122867.1

(22) Date of filing: 24.12.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC

NL PT SE

Designated Extension States:

AL LT LV MK RO SI

(30) Priority: 27.12.1996 JP 356748/96

(71) Applicant:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Kadoma-shi, Osaka-fu (JP)

(72) Inventors:

- Ohta, Gen-Ichiro
Ebina-shi, Kanagawa (JP)

- Inogai, Kazunori
Yokohama-shi, Kanagawa (JP)
- Sasaki, Fujio
Yokohama-shi, Kanagawa (JP)
- Sudo, Hiraoki
Yokohama-shi, Kanagawa (JP)

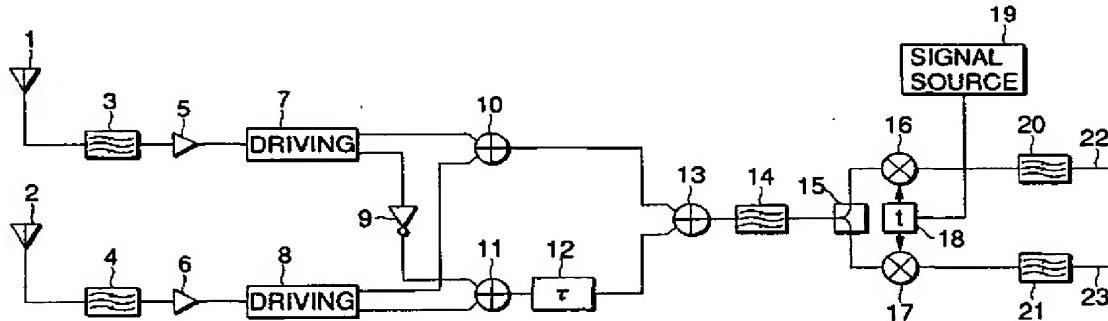
(74) Representative:
Grünecker, Kinkeldey,
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Receiving circuit

(57) A receiving circuit includes a first antenna 1, a second antenna 2, units 10 and 11 for generating a sum signal or a difference signal from signals of two paths received by the respective antennas, a unit 12 for giving delay to either an output of the sum signal generating unit or an output of the difference signal generating unit, a unit 13 for summationally combining an output of the delay unit and the signal of the not-delayed path, a desired-wave pass filter unit 14 for receiving an output of the summationally combining unit, a dividing unit 15

for receiving an output of the desired-wave pass filter unit, an orthogonal detection unit 16-19 for receiving an output of the dividing unit, and a filter unit 20 and 21 for receiving an output of the orthogonal detection unit to extract a base band signal therefrom, wherein the receiving path including the summationally combining unit and the following are made into one path to thereby attain miniaturization and low power consumption.

FIG.1



EP 0 851 605 A2

Description**BACKGROUND OF THE INVENTION**5 **1. Field of the Invention**

The present invention relates to a receiving circuit of a communication equipment, and particularly relates to a receiving circuit in which superior stability in received signal strength can be obtained.

10 **2. Description of the Related Art**

Conventional receivers of communication equipments almost have a space diversity function using a plurality of antennas in order to reduce the influence of fading.

Conventionally, a receiving circuit in a space diversity path shown in Fig. 9 is known. The configuration and principle 15 of the receiving circuit of a first conventional example will be described below with reference to Fig. 9.

In Fig. 9, an arriving radio wave induces a high-frequency signal in each of antennas 201 and 202. The induced signals pass through reception filters 203 and 204 respectively, and are supplied to first-stage reception amplifiers 205 and 206 so as to be amplified respectively. These outputs are supplied to frequency converters 207 and 208 so as to be subjected to frequency-reducing conversion, converted into intermediate-frequency band signals. These intermediate-frequency band signals are supplied to intermediate-frequency amplifiers 211 and 212 through filters 209 and 210 for eliminating unnecessary signals. The outputs of the amplifier 211 and 212 are supplied to detection circuits 215 and 216 through channel filters 213 and 214 for making only desired-frequency signals pass therethrough. The results of the detection circuits 215 and 216 are compared with each other in a comparison circuit 217, and a stronger signal in received signal strength is selected as an output 218. A diversity function is thus realized. A local frequency oscillator 219 supplies a local oscillation frequency signal to the frequency converters 207 and 208 in common.

That is, the above-mentioned first conventional example is constituted by two paths of receiving circuits which are independent of each other perfectly, and a common local signal circuit designed so as to make signal purity and phase uniform. An output is obtained by selection or combination of the two paths of received signals demodulated by these perfectly independent receiving circuits.

30 However, in the receiving circuits in the space diversity path in the above-mentioned first conventional example, not only the two independent receiving circuits consume power, but also their constituent parts increase the equipment volume. In addition, it is necessary to make the performance of the two paths of the receiving circuits equal to each other. Therefore, a second conventional example improving the above-mentioned first conventional example as shown in Fig. 10 has been known. Fig. 10 shows a spectrum spread communication diversity receiver disclosed in JP-A-7-87057, as 35 the second conventional example. In Fig. 10, the spectrum spread communication diversity receiver is constituted by antennas 313 and 314, filters 315 and 316, amplifiers 317 and 318, a delay circuit 319, a combination circuit 320, a matched filter correlator 321, a phase detector 322, a delay circuit 323, a combination circuit 324, and a data demodulator 325.

The antenna 313 and the antenna 314 are made apart from each other by a distance of $\lambda/3$ or more, so that there 40 is substantially no correlation between an SS received signal S5(t) from the antenna 313 side and an SS received signal S6(t) from the antenna 314 side. The filters 315 and 316 eliminate signals in any band other than the signals S5(t) and S6(t). The amplifiers 317 and 318 amplify the signals S5(t) and S6(t).

The delay circuit 319 delays an output S8(t) of the amplifier 318, while the delay time τ is set to $\tau \geq \tau_a$ in the condition 45 that $\tau \geq$ one chip length of PN code, and τ_a designates the maximum delay time of a reflected wave which is influential on a direct wave. The combination circuit 320 combines an output S7(t) of the amplifier 317 and an output S9(t- τ) of the delay circuit 319. The combined SS received signal is separated in the time domain on the basis of the correlative operation with reference PN code performed in the correlator 321.

The reason why the delay is given by the delay circuit 319 is that the SS signal received on the antenna 313 side and the SS signal received on the antenna 314 side which are combined by the combination circuit 320 are separated 50 in the time domain as correlative spike by the correlator 321 to thereby eliminate the interference between the SS signals of the antenna 313 side and of the antenna 314 side.

Then, in the SS signal received on the antenna 313 side, most of combined correlative spikes are suppressed when the difference in delay time between the direct wave and the reflected wave is within one chip length of PN code and the difference in phase between carriers in the correlative spikes outputted from the correlator for the respective 55 received signals is 180° (reverse phase). However, because the SS signal received on the antenna 314 side is not correlative with that of the antenna 313 side, a received signal with independent parameters are obtained. For example, if the above-mentioned difference in phase between carriers in the correlative spikes is 0° (in-phase), the combined correlative spikes are hardly suppressed.

[0011]

In such a state, if combination is performed under the condition of giving delay (by 4 chip length of PN code herein) to the SS signal received on the antenna 314 side, the correlative spikes are prevented from being suppressed by multi-path, so that it is possible to improve the S/N ratio of the received SS signals, and it is possible to improve the performance of data demodulation.

In addition, in this conventional example, the correlative output of the correlator 321 is delayed and detected by the phase detector 322 in order to more improve the performance of data demodulation. Then, in the phase detector 322, detection is performed after multiplying a signal passing through the delay circuit with a delay of one data bit T with an original signal, and the multiplied signal is made to pass through a low pass filter so as to obtain an output.

This delay detection output divides the correlative output of a base band into two divisions. One of the two divisions is delayed in the delay circuit 323, and combined with the other in the combination circuit 324 again. Then, all the delay circuits are set to have an equal delay time. The output of the combination circuit 324 is supplied to the data demodulator 325. With this configuration, two SS signals $S10(t)$ and $S11(t-\tau)$ received on the antennas 313 side and on the antenna 314 side respectively are suppressed by multi-path, and made into a signal $S12(t)$ by the combination of their correlative peaks, so that its correlative peak value is V_1+V_2 when the peak values of the respective signals are V_1 and V_2 respectively. The S/N ratio is more improved, so that it is possible to improve the performance of data demodulation.

According to the above-mentioned second conventional example, the two paths of received signals are made into a single path in the combination circuit 320 and the following means, so that there is an effect to reduce the number of parts of the receiving circuits.

However, in the above-mentioned second conventional example, the canceling operation of carriers themselves between the two paths of received signals is left as it is, so that the output of the combination circuit 320, that is, the input signal of the matched-filter correlator 321 is attenuated with a high probability.

The aspect of this attenuation will be explained with reference to Figs. 11A to 11D. Figs. 11A to 11D show an example of a diversity effect in the second conventional example shown in Fig. 10. Fig. 11A designates a signal referred to as a so-called chip which is a product of a spread signal and an information signal of a spectrum spread communication signal lent to this receiver. Fig. 11B designates signals received by receiver antennas in the case of a modulation output in which a chip signal is modulated into 4 times of carrier frequency an a modulation wave by way of example. A portion (b-1) of Fig. 11B designates a signal received by an antenna 1, while a portion (b-2) of Fig. 11B a signal received by an antenna 2. Because the antenna 1 and the antenna 2 are made to be separated from each other by a distance of 1/3 or more of the wave length of a carrier in the second conventional example, the distance is set to one wave length herein, and the difference in phase ϕ is made 2π . Fig. 11C designates the case where a signal path received from the antenna 1, that is, a signal of a branch 1, and a signal path received from the antenna 2, that is, a signal of a branch 2 are added to each other by a differential amplifier, that is, subtracted from each other. Fig. 11D designates the case where the signal of the branch 1 side is simply combined with the delayed signal of the branch 2 side in accordance with the second conventional example.

In Figs. 11A to 11D, in order to make the explanation of the problem clear, it is assumed that there arises no canceling operation between arriving waves caused by multi-path fading in the antenna 1 and the antenna 2. It is understood from Fig. 11C that when the signals of the branches are added or subtracted simply, an adding/canceling operation of the signals similar to the canceling operation caused by multi-path fading arising on the antenna ends arises between the branches, so that there is a high probability that the time when the received signals disappear occurs frequently. In addition, it is understood from Fig. 11D that although there to some effect obtained by delaying a signal, the time of signal disappearance remains as it is with considerable frequency.

On the contrary, in the first conventional example, the signal superior in received conditions is selected from the branch 1 and the branch 2 every moment, or adaptive combination of signals is performed so as to eliminate the time when the received signals disappear. Therefore, it is impossible in the second conventional example to obtain a space diversity effect equal to that in the first conventional example.

SUMMARY OF THE INVENTION

The present invention has been made to solve the foregoing conventional problems, and it is an object of the present invention to provide a receiving circuit in which superior stability in received signal strength can be obtained.

In order to solve the above problem, according to the present invention, there is provided a receiving circuit comprising means for generating a sum signal or a difference signal from signals of two paths received by the respective antennas, means for giving delay to either an output of the sum signal generating means or an output of the difference signal generating means, means for summationally combining an output of the delay means and the signal of the not-delayed path, a desired-wave pass filter means for receiving an output of the summationally combining means, a dividing means for receiving an output of the desired-wave pass filter means, an orthogonal detection means for receiving

an output of the dividing means, and a filter means for receiving an output of the orthogonal detection means to extract a base band signal therefrom, wherein the receiving path including the summationally combining means and the following are made into one path.

With this configuration, not only a space diversity function similar to that of the first conventional example having two receiving paths independently can be realized, but also the size and the power consumption can be reduced.

According to a first aspect of the invention, there is provided a receiving circuit comprising a first antenna, a second antenna, means for generating a sum signal or a difference signal from signals of two paths received by the respective antennas, means for giving delay to either an output of the sum signal generating means or an output of the difference signal generating means, means for summationally combining an output of the delay means and the signal of the not-delayed path, a desired-wave pass filter means for receiving an output of the summationally combining means, a dividing means for receiving an output of the desired-wave pass filter means, an orthogonal detection means for receiving an output of the dividing means, and a filter means for receiving an output of the orthogonal detection means to extract a base band signal therefrom, wherein the receiving path including the summationally combining means and the following are made into one path. Accordingly, there is obtained an effect that the size and the power consumption can be reduced.

According to a second aspect of the invention, there is provided a receiving circuit according to the first aspect of the invention, wherein means for subtractively combining the output of the delay means and the signal of the not-delayed path is provided in place of the means for summationally combining the output of the delay means and the signal of the not-delayed path. Accordingly, there is obtained an effect that noise from a power supply path or distortion in the same kind in the reception input circuit can be reduced.

According to a third aspect of the invention, there is provided a receiving circuit according to the first aspect of the invention, further comprising an intermediate-frequency converting means constituted by an intermediate-frequency local oscillation signal source, a frequency conversion mixer and an intermediate-frequency band filter is provided, wherein the output of the means for summationally combining the output of the delay means and the signal of the not-delayed path or the output of the means for subtractively combining the output of the delay means and the signal of the not-delayed path is applied to the intermediate-frequency converting means to thereby make the receiving path including the intermediate-frequency band stage and the following into one path. Accordingly, there is obtained an effect that the influence of phase error produced in the generation of the sum signal or the difference signal can be reduced.

According to a fourth aspect of the invention, there is provided a receiving circuit according to the first aspect of the invention, wherein individual frequency converting means are provided for the signals of the two paths obtained from the respective antennas, and the means for generating a sum signal and a difference signal from the signals of the two paths obtained by the respective frequency converting means are provided in an intermediate-frequency band to make the receiving path including the intermediate-frequency band stage and the following into one path. Accordingly, there is obtained an effect that not only the phase accuracy based on the circuit wiring length can be prescribed by the intermediate-frequency band, but also power consumption can be reduced.

According to a fifth aspect of the invention, there is provided a receiving circuit according to the first aspect of the invention, wherein three or more antennas are provided to constitute three or more branches, and that means for generating a sum signal and a difference signal upon signals from the three or more paths, so that means for giving delay to all but one of outputs of the sum signal generating means or outputs of the difference signal generating means, means for summationally or subtractively combining an output of the delay means and the signal of the not-delayed path are provided to thereby make the receiving path including the combination means and the following into one path. Accordingly, there is an effect that the size and the power consumption can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

- Fig. 1 is a diagram illustrating the configuration of a receiving circuit according to a first embodiment of the present invention;
 Figs. 2A to 2F are diagrams for explaining the operation in the first embodiment of the present invention;
 Figs. 3A and 3B are diagrams for explaining the effect in the first embodiment of the present invention;
 Fig. 4 is a diagram illustrating the configuration of a receiving circuit according to a second embodiment of the present invention;
 Fig. 5 is a diagram for explaining the effect in the second embodiment of the present invention;
 Fig. 6 is a diagram illustrating the configuration of a receiving circuit in a third embodiment of the present invention;
 Fig. 7 is a diagram illustrating the configuration of a receiving circuit in a fourth embodiment of the present invention;
 Fig. 8 is a diagram illustrating the configuration of a receiving circuit in a fifth embodiment of the present invention;
 Fig. 9 is a diagram illustrating the configuration of a first conventional receiving circuit having two receiving paths;
 Fig. 10 is a diagram illustrating the configuration of a second conventional receiving circuit in which the receiving

paths are reduced; and

Figs. 11A to 11D are diagrams for explaining the operation of the second conventional receiving circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5

A description will be given in more detail of preferred embodiments of the invention with reference to Figs. 1 to 8.

(First Embodiment)

10 Fig. 1 shows a configuration of a receiving circuit in a first embodiment of the present invention. In Fig. 1, the receiving circuit is constituted by an antenna 1 for a branch 1 of space diversity, an antenna 2 for a branch 2 of space diversity, a filter 3 for receiving an arriving wave signal obtained by the antenna 1 and extracting a signal component in a desired band, a filter 4 for receiving an arriving wave signal obtained by the antenna 2 and extracting a signal component in a desired band, an amplifier 5 for amplifying the desired-band signal obtained by the filter 3, an amplifier 6 for amplifying the desired-band signal obtained by the filter 4, means 7 for dividing the desired-band signal of the branch 1 side into two paths, means 8 for dividing the desired-band signal of the branch 2 side into two paths, means 9 for inverting a polarity or shifting a phase by 180 degrees, means 10 for combining a signal from the dividing means 7 and a signal from the dividing means 8, means 11 for combining a signal from the polarity inverting or 180-degrees phase shifting means 9 and a signal from the dividing means 8, means 12 for receiving and delaying the output of the combining means 10, means 13 for receiving the output of the combining means 11 and the output of the delay means 12 and combining the received outputs, a filter means 14 for receiving the output of the combining means 13 and limiting the received output in a desired signal band, means 15 for receiving the output of the filter means 14 and dividing the received output, a first multiplier 16 constituting an orthogonal detector, a second multiplier 17 constituting the orthogonal detector, a distributor 18 including a $\pi/2$ phase shifter so as to give a phase shift to one of the orthogonal detectors and feed a detection local oscillation signal to the orthogonal detector, a signal source 19 of the local oscillation signal fed to the distributor 18, a filter 20 for receiving the output of the first multiplier 16 and extracting a base band signal, a filter 21 for receiving the output of the second multiplier 17 and extracting a base band signal, on output terminal 22 from which the output of the first base band signal obtained by orthogonal detection is obtained, and an output terminal 23 from which the output of the second base band signal obtained by orthogonal detection is obtained.

30 The operation of the above configuration will be described with reference to Figs. 2A to 2F. Figs. 2A and 2B are similar to Figs. 11A to 11D. Fig. 2A designates a signal referred to an so-called chip which is a product of a spread signal and an information signal of a spectrum spread communication signal transmitted to this receiver. Fig. 2B designates a signal received by the receiver antennas in the case of a modulation output obtained by using the chip signal as a modulated wave and modulating the chip signal to a four-times carrier frequency by way of example.

35 A portion (b-1) of Fig. 2B designates a signal received by the antenna 1, and a portion (b-2) of Fig. 2B designates a signal received by the antenna 2. The antenna 1 and the antenna 2 are set to 1 wave length in view of the carrier, and the phase difference ϕ between the antenna 1 and the antenna 2 is made 2π . Fig. 2C designates the case where subtraction is made between the reception path received by the antenna 1, that is, the signal of the branch 1, and the reception path received by the antenna 2, that is, the signal of the branch 2. Fig. 2D designates the case where the signal of the branch 2 side is delayed in accordance with the above-mentioned second conventional example so as to combine this signal and the signal of the branch 1 side by simple addition. Fig. 2C designates the case where simple addition is made between the reception path received by the antenna 1, that is, the signal of the branch 1, and the reception path received by the antenna 2, that is, the signal of the branch 2. Fig. 2D designates the case where simple subtraction is made. Fig. 2D corresponds to Fig. 11C. Fig. 2E shows that the result of the simple subtraction in Fig. 2D is delayed by one chip time. Fig. 2F shows that Figs. 2C and 2E are combined summationally.

Also in Figs. 2A to 2F, in order to make the description clear, it is assumed that there arises no canceling operation between arriving waves caused by multi-path fading in the antenna 1 and the antenna 2.

It is understood from Fig. 2F that the canceling operation between signals of the branches is reduced, so that the time when the signals disappear can be reduced extremely. This will be explained by numerical expressions. Respective parameters in the numerical expressions are shown in Figs. 3A and 3B.

Fig. 3A shows parameters in the first embodiment of the present invention, and Fig. 3B shows parameters in the above-mentioned second conventional example.

Refer to the path in the first embodiment of the present invention as sum-difference delay combination, and refer to the path in the above-mentioned second conventional example as simple delay combination.

55 When the not-delayed and delayed signals of the branch 1 are represented by A and A(τ) respectively, and the not-delayed and delayed signals of the branch 2 are represented by B and B(τ) respectively, outputs in the respective combinations can be expressed by:

(sum-difference delay combination) = $A-B+A(\tau)+B(\tau)$ (simple delay combination) = $A+B(\tau)$.

- 5 First, the conditions when the output of the simple delay combination which is the second conventional example becomes zero will be examined.

It is apparent that the output becomes zero if the amplitudes of the branch 1 and the branch 2 are equal, and the phase difference between the two branches is 180 degrees at the time of generating a sum signal. That is, the signal disappears at the output terminal when established is:

10 $|A|=|B(\tau)|=|B|$

$$\text{angle}(A)-\text{angle}(B(\tau))=(2n+1)\pi.$$

- 15 The phase difference $(2n+1)\pi$ between A and $B(\tau)$ is the sum of the delay time τ and the phase difference between the two branches. Therefore, the phase between the branches changes variously under the practical environment, so that the moment satisfying this condition appears in a high frequency.

Although it can be considered that this condition is prevented from being established by controlling the delay time of the delay circuit adaptively, it is almost impossible to do so under the moving situations of mobile communication.

- 20 When the addition of equipments required for such control and the increase of power consumption are taken into consideration, such control can be judged not practical.

Next, it will be confirmed whether the signal disappears in the path of the present invention or not when the above condition is established.

- 25 The sum-difference delay combination will be considered on the same divisional components as the component in the second conventional example, that is, the portion of $A+B(\tau)$, and the unique component, that is, the portions of $A(\tau)-B$. Under this condition,

the same component as that in the second conventional example: $A+B(\tau) \rightarrow 0$, but
the unique component of the present invention: $A(\tau)-B \rightarrow 2A$ or $2B$ ($\neq 0$). Therefore, totally,

30 (sum-difference delay combination) = $2A$ ($\neq 0$).

It is therefore understood that an output signal can be ensured without disappearing in the present invention even under the condition in which the signal disappears in the second conventional example.

- 35 Next, it will be considered whether the output disappears or not under peculiar conditions in the path of the present invention.

That is, the case where the sum-difference delay combination becomes zero can be expressed by:

(sum-difference delay combination) = $A-B+A(\tau)+B(\tau)$.

- 40 When the carrier frequency is represented by ω_0 , the above expression can be expressed by the following expression (1).

$$A-B+A(\tau)+B(\tau) = A_0[\cos\omega_0(t)+\cos\omega_0(t+\tau)]+B_0[-\cos\omega_0(t)+\cos\omega_0(t+\tau)] \quad (1)$$

- 45 wherein $A_0 \geq 0$, $B_0 \geq 0$.

In order to make the value of this expression take zero, the first term and the second term must cancel each other, or both the first and second terms must take zero at the same time, so long as A_0 and B_0 are not zero.

First, in order to confirm whether the first term and the second term cancel each other or not, the following expression (2) is obtained by combining like terms.

50 $A_0[\cos\omega_0(t)+\cos\omega_0(t+\tau)]+B_0[-\cos\omega_0(t)+\cos\omega_0(t+\tau)] = (A_0-B_0)\cos\omega_0(t)+(A_0+B_0)\cos\omega_0(t+\tau) \quad (2)$

In order to make the value of this expression (2) take zero in the periodical level of the carrier, that is, takes zero independently of the value of time t ,

$$(A_0-B_0)\cos\omega_0(t)=0, \text{ and at the same time } (A_0+B_0)\cos\omega_0(t+\tau)=0.$$

Because the first term and the second term must be zero at the same time independently of the value of cosine which is a function of time t ,

$$A_0 - B_0 = 0, \text{ and at the same time } A_0 + B_0 = 0 \quad (3)$$

must be established.

Although A_0 and B_0 can take zero individually, there is no possibility that they take zero at the same time. This is because it is a premise in space diversity that the antennas are disposed so that A_0 and B_0 do not take zero at the same time.

That is, $A_0 + B_0 = 0$ is not established. Therefore, the above expression (3) is not established.

Next, the case where the first term and the second term take zero independently in the expression (1) will be examined. Then, the expression (1) is transformed into the following expression (4) for the examination.

10

$$\begin{aligned} & A_0[\cos\omega_0(t)+\cos\omega_0(t+\tau)]+B_0[-\cos\omega_0(t)+\cos\omega_0(t+\tau)] \\ &= 2A_0\cos\omega_0(t+\tau/2)\cos\omega_0(\tau/2)+2B_0[\sin\omega_0(t+\tau/2)\sin\omega_0(\tau/2)] \end{aligned} \quad (4)$$

15 Then, in order to make the first term and the second term take zero at the same time independently of the values of cosine or sine which are functions of time t in the same manner as mentioned above,

20

$$2A_0\cos\omega_0(\tau/2)=0, \text{ and at the same time } 2B_0\sin\omega_0(\tau/2)=0 \quad (5)$$

must be established.

Because A_0 or B_0 which are inputs of the antennas can take zero individually, there is an adequate possibility that either amplitude of the first term or the second term in the above expression (5) becomes zero. Then, when zero is taken in the term in which the amplitude is not zero,

25

$$\cos\omega_0(\tau/2)=0, \text{ or } \sin\omega_0(\tau/2)=0 \quad (6)$$

must be established. That is,

30

$$\omega_0(\tau/2)=(2n+1)\pi, \text{ or } \omega_0(\tau/2)=2n\pi. \quad (7)$$

To sum up,

$$\omega_0\tau=n\pi. \quad (8)$$

35

It is understood therefrom there is a possibility that the output disappears only when the delay time τ in the delay circuit takes an integer multiple of the phase difference of 180 degrees to the carrier frequency.

However, this makes it apparent that the above expression (1) does not take zero independently of the arrangement of the antenna 1 and the antenna 2 or the state of multi-path fading if the delay time τ in the delay circuit is not set to any integer multiple of the phase difference of 180 degrees to the carrier frequency.

40

To sum up, in the second conventional example, the conditions for the output to disappear include the arrangement of the antenna 1 and the antenna 2 or the state of multi-path fading. It is therefore almost impossible to set the delay time of the delay circuit to a satisfactory value. Accordingly, the output has disappeared in a high frequency.

On the other hand, in the present invention, the conditions for the output to disappear are controlled by setting the delay time τ of the delay circuit to an integer multiple of the phase difference of 180 degrees to the carrier frequency.

45

Accordingly, the disappearance of the output in the above dispute can be avoided perfectly by preventing this delay time from taking any integer multiple of the phase difference of 180 degrees to the carrier frequency.

50

Because the delay time of the delay circuit may be set by the unit of chip time, the chip time is basically independent of the carrier frequency. Further, the chip time is so much longer than the period of the carrier frequency that the deterioration of the accuracy to the period of the carrier, that is, the deterioration of the synchronizing accuracy influenced by the time quantity shifted from an integer multiple of the phase difference of 180 degrees is hardly generated, so that it is insignificant.

Therefore, desired setting of the delay time of the delay circuit in the present invention can be realized without any influence on others.

55

From the above description, in the first of the present invention, in comparison with the above-mentioned first conventional example, the receiving path of the combination circuit 13 and the following means can be made into one path, so that it is apparent that it is possible to obtain economical effects such as reducing circuit parts corresponding to one path, reducing the size of the apparatus, reducing the power consumption, reducing the cost, and so on, and in the performance, it is possible to obtain an effect to solve such a problem belonging to the above-mentioned second conven-

tional example that a signal output frequently disappears or attenuates.

(Second Embodiment)

5 Fig. 4 shows a receiving circuit according to a second embodiment of the present invention. In Fig. 4, the constituents from the reference numeral 1 to the reference numeral 23 are the same as those in the first embodiment shown in Fig. 1, except the reference numerals 110, 111 and 113.

The receiving circuit in the second embodiment of the present invention includes means 110 for subtractively combining a signal from the means 7 for dividing a desired-band signal of the branch 1 side into two paths and a signal from the means 8 for dividing a desired-band signal of the branch 2 side into two paths, means 111 for subtractively combining a signal from the means 9 for inverting polarity or shifting phase by 180 degrees and a signal from the means 8 for dividing the desired-band signal of the branch 2 side into two paths, means 12 for receiving the output of the subtractively combining means 111 and delaying the received output, and means 113 for receiving the output from the subtractively combining means 110 and the output of the delay means 12 and subtractively combining the received outputs.

10

15 The output from the subtractively combining means 113 is supplied to the filter means 14 for limiting the output to a desired signal band.

The operation of the receiving circuit thus structured according to the second embodiment of the invention will be described with reference to Fig. 5.

Fig. 5 shows the state where noises mixed into the power supply or signal lines in Fig. 4. In Fig. 5, n1 designates 20 a noise mixed into constituent parts constituted by the filter 3, the amplifier 5 and the dividing means 7 for the branch 1 of space diversity; n2 designates a noise mixed into constituent parts constituted by the filter 4, the amplifier 6 and the dividing means 8 for the branch 2 of space diversity; n3 designates a noise mixed into the combining means 110 and a signal path thereof; and n4 designates a noise mixed into the combining means 111 and a signal path thereof.

Because the noise in the output of the dividing means 7 is n1 and the noise in the output of the dividing means 8 is n2, a noise appears in the output of the subtractively combining means 110 as follows:

$$n1-n2+n3.$$

Similarly, a noise appears in the output of the subtractively combining means 111 as follows:

$$n1-n2+n4.$$

Because the polarity inverting means 9 is disposed so as to be close to an output terminal of the dividing means 7 on the circuit in Fig. 5, it is considered that the noise n1 also appears in the output terminal of the polarity inverting means 35 9.

Therefore, a noise appears in the output of the combining circuit 113 for receiving the output from the subtractively combining means 110 and the output from the subtractively combining means 111 as differential inputs as follows:

$$(n1-n2+n3)-(n1-n2+n4).$$

40 Then, if the circuits of the branch 1 and the branch 2 are under the same conditions to noises for the reason why they are equivalent geometrically or for any other reasons,

$$n1=n2, \text{ and } n3=n4$$

45 are established.

Then, the output of the combining circuit 113 is:

$$(n1-n2+n3)-(n1-n2+n4)=(n1-n1)(-n2+n2)+(n3-n4)=0$$

50 That is, in the configuration according to the second embodiment of the invention, it is apparent that the noises mixed in the inside of the apparatus can be canceled so as to be reduced if the arrangements and structures of the branches are the same.

Consequently, it is possible to obtain an effect to reduce noises mixed from the neighborhood even if two paths of 55 branch signals are passed through a single signal processing path.

(Third Embodiment)

Fig. 6 shows a receiving circuit according to a third embodiment of the present invention. In Fig. 6, the constituents from the reference numeral 1 to the reference numeral 23 are the same as those in the second embodiment shown in Fig. 4. In the third embodiment of the present invention, an intermediate-frequency band local oscillation signal source 24, a frequency converting mixer 25 for receiving the output of the subtractively combining means 113 and the above-mentioned intermediate-frequency band local oscillation signal, and an intermediate-frequency band filter 114 are added to the configuration of the above-mentioned second embodiment.

In the above-mentioned first or second embodiment of the invention, summationally and subtractively combined and delayed signals between the branches are supplied to an orthogonal detector directly in a radio frequency band. However, in this path, the orthogonal detector and the following means must play a part as a channel filter. This is because the filters 3 and 4 close to the antennas 1 and 2 must pass all the frequency channels, and, therefore, they cannot be made to be a filter only for passing a desired frequency channel.

That is, all the circuit to the orthogonal detector is required to have a broad-band performance to pass all the channels, the local oscillation signal source 19 to the orthogonal detector must be switched in accordance with a desired channel frequency, and the filters 20, 21 and so on following the detector are required to have a function to eliminate adjacent waves in a wide range.

In addition, because the rate of generation of saturated state in the circuit dynamic range is increased due to the adjacent waves and so on, so-called signal suppression appears on signals in the desired channel.

In the third embodiment of the invention, a channel filter function is held by providing an intermediate-frequency converting means constituted by the intermediate-frequency band local oscillation signal source 24, the frequency converting mixer 25, and the intermediate-frequency band filter 114, so that the disadvantage to require the following circuits such as the orthogonal detector and so on to have a channel filter function is eliminated. By switching the frequency of the intermediate-frequency band local oscillation signal source 24, a desired channel signal in easily tuned in the intermediate-frequency band, so that it is possible to establish a channel filter function by the intermediate-frequency band filter 114 having only single-channel width.

As a result, the following circuits, for example, circuits for the orthogonal detector may have only a narrow band performance to pass a single channel. Accordingly, the local oscillation signal source 19 for the detector and the following means can be made to have a fixed frequency, and the filters 20, 21 and so on following the detector may have only a narrow-range pass band. In addition, the generation of saturated state in the circuit dynamic range caused by desired waves and so on is reduced, so that it is possible to obtain an effect to reduce signal suppression on signals of a desired channel.

(Forth Embodiment)

Fig. 7 shows the configuration of a receiving circuit in a fourth embodiment of the present invention. In Fig. 7, the constituents of the reference numerals from 1 to 23 are the same as those in the second embodiment shown in Fig. 4.

In the fourth embodiment of the present invention, an intermediate-frequency band local oscillation signal source 24, a frequency converting mixer 25 for receiving the output of the amplifier 5 and the above-mentioned intermediate-frequency band local oscillation signal, a frequency converting mixer 26 for receiving the output of the amplifier 6 and the above-mentioned intermediate-frequency band local oscillation signal, an amplifier 27 for receiving the above-mentioned intermediate-frequency band local oscillation signal and supplying its output to the frequency converting mixer 25, and an amplifier 28 for receiving the above-mentioned intermediate-frequency band local oscillation signal and supplying its output to the frequency converting mixer 26 are added to the configuration of the above-mentioned second embodiment of the invention.

In the first, second or third embodiment of the invention, the frequency band to generate a sum and a difference of respective branch signals is in a radio frequency band. Therefore, when the radio frequency is, for example, 1 GHz, the difference of circuit wiring length between the branches has to be set to 1.67 mm or less in order to make the phase difference between the branches 3 degrees or less. That is, the degree of freedom in designing circuit wiring decreases extremely. At the same time, a severe restriction becomes required in the change of performance of parts due to a temperature change or the like.

In order to solve such a problem with the first to third embodiments, the fourth embodiment of the present invention is designed so that sum and difference signals are obtained after lowering the respective branch signals to an intermediate-frequency band.

In Fig. 7, the output of the amplifier 5 for amplifying the received signal of the branch 1 is supplied to the frequency converting mixer 25, and converted into an intermediate frequency. The output of the amplifier 6 for amplifying the received signal of the branch 2 is supplied to the frequency converting mixer 26, and converted into the intermediate frequency. The frequency converting mixers 25 and 26 receive an intermediate-frequency band local oscillation signal

from the intermediate-frequency band local oscillation signal source 24 through the amplifiers 27 and 28 respectively. A desired channel can be selected by changing-over the intermediate-frequency band local oscillation frequency from the intermediate-frequency band local oscillation signal source 24.

The output of the frequency converting mixer 25 is supplied to the means 7 for dividing the output into two paths, while the output of the frequency converting mixer 26 is supplied to the means 8 for dividing the output into two paths. The succeeding operation is the same as that in the above-mentioned second embodiment. Although all the means from the dividing means 7 and 8 to the multipliers 16 and 17 of the orthogonal detector are in the radio frequency band in the second embodiment of the invention, however, they are in a intermediate-frequency band in the fourth embodiment of the invention.

As a result, the phase accuracy depending on the length of wiring of the circuits for generating sum and difference signals and the circuits for polarity inversion or signal delay may be defined in accordance with the intermediate frequency.

On the assumption that the intermediate frequency is 100 MHz, it will go well if the circuit wiring length is set to 16.7 mm or less in order to make the phase difference between sum and difference signals be not larger than 3 degrees.

Accordingly, the degree of freedom in designing the circuit wiring has a tolerance ten times as large as that in the case of the radio frequency band. In addition, because all the means from the dividing means 7 and 8 to the multipliers 16 and 17 of the orthogonal detector may be in the intermediate-frequency band, there is another effect that semiconductor devices are designed easily and the power consumption can be reduced on a large scale.

20 (Fifth Embodiment)

Fig. 8 shows the configuration of a receiving circuit in a fifth embodiment of the present invention. In Fig. 8, the constituents from the reference numeral 13 to the reference numeral 23 are the same as those in the first embodiment shown in Fig. 1. In addition, the constituents from the reference numeral 1 to the reference numeral 12 are also the same as those in the first embodiment of the invention except for the suffixed provided in the receiving circuit.

In the fifth embodiment of the present invention, the constituents of the reference numerals from 1 to 12 in the first embodiment of the invention are designed so as to have a plurality of constituent parts. That is, there are provided antennas 1a, 1b and 1c for respective branches of space diversity, filters 3a, 3b and 3c for receiving arriving wave signals obtained by the antennas 1a, 1b and 1c and extracting a signal component in a desired band, amplifiers 5a, 5b and 5c for amplifying the desired-band signals obtained by the filters 3a, 3b and 3c, means 7a, 7b and 7c for dividing the desired-band signals from the respective branches into three paths, means 9a, 9b and 9c for inverting polarity or shifting phase by 180 degrees, means 11a, 11b and 11c for combining a signal obtained from one of the dividing means 7a, 7b and 7c and signals obtained from two of the polarity inverting or 180-degrees phase shifting means 9a, 9b and 9c, means 12b for receiving the output of the combining means 11b and delaying the received output by τ , and means 12c for receiving the output of the combining means 11c and delaying the received output by 2τ .

The operation of the receiving circuit in the fifth embodiment of the invention thus configured will be described with reference to Fig. 8.

When a signal of the branch 1 is designated by A1, a signal of the branch 2 is by A2, and a signal of the branch 3 is by A3, the outputs of the combining circuits 11a, 11b and 11c are respectively expressed by:

$$40 \quad (\text{output of the combining circuit } 11a) = A1+A2-A3$$

$$(\text{output of the combining circuit } 11b) = -A1+A2+A3$$

$$45 \quad (\text{output of the combining circuit } 11c) = A1-A2+A3.$$

When a signal delayed by the delay circuit 12b is expressed by adding a suffix (τ_1), and a signal delayed by the delay circuit 12c is expressed by adding a suffix (τ_2), the output of the combining circuit 13 is expressed by the following expressions (9) and (10).

50

55

(output of the combining circuit) = A₁+A₂-A₃-

5 A₁(τ₁)+A₂(τ₁)

+ A₃(τ₁)+A₁(τ₂)-

10 A₂(τ₂)+A₃(τ₂) ... (9)

= { A 1 -

15 A₁(τ₁)+A₁(τ₂)}+{A₂+A₂(τ₁)-

A₂(τ₂)}+{A₃+A₃(τ₁)+A₃(τ₂)} ... (10)

The expression (9) means that only one in any of groups in which the delay quantity is made the same in the combination of the respective branches is inverted in its polarity, that is, is shifted in its phase by 180 degrees, and a branch different by group is inverted in its polarity, that is, is shifted in its phase by 180 degrees.

This means that the signals of the branches 1, 2 and 3 are prevented from disappearance arising when they are combined into a single signal.

The expression (10) means that in the case where signals in the same branch are subjected to a plurality of delays and then combined so that the signals disappear, it can be prevented that all the signals of the branch disappear if combination of addition and subtraction differently by branch is carried out.

This will be made clearer by use of numerical expressions.

Similarly to the case of two branches, it will be examined whether the output disappear or not under peculiar conditions in the fifth embodiment of the invention.

That is, when the sum-difference delay combination takes zero, the above-mentioned expression (10) can be expressed by the following expression (11) on the assumption that the carrier frequency is expressed by ω₀.

$$\begin{aligned}
 & \{A_1-A_1(\tau_1)+A_1(\tau_2)\}+[A_2+A_2(\tau_1)-A_2(\tau_2)]+[-A_3+A_3(\tau_1)+A_3(\tau_2)] \\
 & =A_{01}\{\cos\omega_0(t)-\cos\omega_0(t+\tau)+\cos\omega_0(t+2\tau)\}+A_{02}\{\cos\omega_0(t)+\cos\omega_0(t+\tau) \\
 & \quad -\cos\omega_0(t+2\tau)\}+A_{03}\{-\cos\omega_0(t)+\cos\omega_0(t+\tau)+\cos\omega_0(t+2\tau)\} \\
 & =0
 \end{aligned} \tag{11}$$

wherein A₀₁≥0, A₀₂≥0, A₀₃≥0

40 In order to make the value of this expression take zero, the first, second and third terms must cancel each other, or take zero at the same time, so long as A₀₁, A₀₂ and A₀₃ are not zero.

First, in order to confirm whether the first, second and third terms cancel each other or not, the expression (10) can be expressed by the following expression (12) obtained by combining like terms.

$$\begin{aligned}
 & \{A_1-A_1(\tau_1)+A_1(\tau_2)\}+[A_2+A_2(\tau_1)-A_2(\tau_2)]+[-A_3+A_3(\tau_1)+A_3(\tau_2)] \\
 & =(A_{01}+A_{02}-A_{03})\cos\omega_0(t)+(-A_{01}+A_{02}+A_{03})\cos\omega_0(t+\tau) \\
 & \quad +(A_{01}-A_{02}+A_{03})\cos\omega_0(t+2\tau) \\
 & =0
 \end{aligned} \tag{12}$$

50

In order to make the value of this expression (12) take zero in the periodical level of the carrier, that is, takes zero independently of the value of time t,

55 (A₀₁+A₀₂-A₀₃)cosω₀(t)=0,

at the same time, (-A₀₁+A₀₂+A₀₃)cosω₀(t+τ)=0, and

EP 0 851 605 A2

at the same time, $(A_{01} - A_{02} + A_{03})\cos \omega_0(t+2\tau) = 0$

must be established.

Because the first, second and third terms must take zero at the same time independently of the value of cosine which is a function of time t ,

$$A_{01} + A_{02} - A_{03} = 0, \quad (13)$$

at the same time, $-A_{01} + A_{02} + A_{03} = 0$, and

at the same time, $A_{01} - A_{02} + A_{03} = 0$

must be established.

The necessary condition for establishing the expression (13) is:

$$A_{01} + A_{02} + A_{03} = 0.$$

Although A_{01} , A_{02} and A_{03} can take zero individually because they are absolute values, there is no possibility that they take zero at the same time. This is because it is a premise in space diversity that the antennas are arranged so that the values do not take zero at the same time. Therefore, $A_{01} + A_{02} + A_{03} = 0$ is established.

Next, the case where the first, second and third terms take zero independently in the expression (11) will be examined. Then, the expression (11) is transformed into the following expression (14) for the examination.

$$\begin{aligned}
 & A_{01}\{\cos \omega_0(t) - \cos \omega_0(t+\tau) + \cos \omega_0(t+2\tau)\} + A_{02}\{\cos \omega_0(t) + \cos \omega_0(t+\tau) - \\
 & \quad \cos \omega_0(t+2\tau)\} + A_{03}\{-\cos \omega_0(t) + \cos \omega_0(t+\tau) + \cos \omega_0(t+2\tau)\} \\
 & = A_{01}(\cos \omega_0(t+\tau)\cos \omega_0(\tau/2) + 1/2[\sin \omega_0(t+\tau/2) + \sin \omega_0(t+3\tau/2)]) \\
 & \quad + \sin \omega_0(\tau/2) + A_{02}(\cos \omega_0(t+\tau/2)\cos \omega_0(\tau/2) + 1/2[\sin \omega_0(t+\tau) \\
 & \quad + \sin \omega_0(t+3\tau/2)])\sin \omega_0(\tau/2) + A_{03}(\cos \omega_0(t+3\tau/2)\cos \omega_0(\tau/2) \\
 & \quad + 1/2[\sin \omega_0(t+\tau/2) + \sin \omega_0(t+\tau)]\sin \omega_0(\tau/2)) \\
 & = A_{01}\{\cos \omega_0(t+\tau)\cos \omega_0(\tau/2) + \sin \omega_0(t+\tau)\sin \omega_0(\tau/2)\cos \omega_0(\tau/2)\} \\
 & \quad + A_{02}\{\cos \omega_0(t+\tau/2)\cos \omega_0(\tau/2) + \sin \omega_0(t+5\tau/4)\sin \omega_0(\tau/2)\cos \omega_0(\tau/2)\} \\
 & \quad + A_{03}\{\cos \omega_0(t+3\tau/2)\cos \omega_0(\tau/2) + \sin \omega_0(t+3\tau/4)\sin \omega_0(\tau/2)\cos \omega_0(\tau/2)\} \\
 & = \cos \omega_0(\tau/2)(A_{01}\{\cos \omega_0(t+\tau) + \sin \omega_0(t+\tau)\sin \omega_0(\tau/2)\} \\
 & \quad + A_{02}\{\cos \omega_0(t+\tau/2) + \sin \omega_0(t+5\tau/4)\sin \omega_0(\tau/2)\} \\
 & \quad + A_{03}\{\cos \omega_0(t+3\tau/2) + \sin \omega_0(t+3\tau/4)\sin \omega_0(\tau/2)\})
 \end{aligned} \quad (14)$$

In order to make the values of the first to third terms of the above-mentioned expression (14) take zero at the same time independently of the values of cosine or sine which are functions of time t ,

$$\cos \omega_0(\tau/2) = 0 \quad (15)$$

$$\tau/2 = (2n+1)\pi.$$

That is,

$$\tau = n\pi. \quad (16)$$

It is apparent that the output may disappear only when the delay time τ in the delay circuit takes an integer multiple of the phase difference of 180 degrees to the carrier frequency.

However, this makes it apparent that the above expression (14), that is, the above expression (11) does not take zero independently of the arrangement of the antenna 1, the antenna 2 and the antenna 3 or the state of multi-path fading unless the delay time τ in the delay circuit is set to any integer multiple of the phase difference of 180 degrees to the carrier frequency.

As is apparent from the above description, it can be the that the receiving circuit in the fifth embodiment of the present invention performs the same operation as the receiving circuit in the above-mentioned first embodiment of the invention basically. Therefore, it is apparent that the space diversity effect of the present invention can be exhibited in the configuration of the fifth embodiment of the invention also in the case where three or more antennas or branches are provided.

In the receiving circuit in the fifth embodiment of the present invention, in comparison with the above-mentioned first embodiment of the invention, the receiving path of the combining circuit 13 and the following means can be made into one path in spite of increasing the number of branches in order to improve the space diversity effect. As a result, as the space diversity effect is more improved, the receiving circuit in the fifth embodiment of the invention can be expected to have a effect higher than the receiving circuit in the first embodiment of the invention.

Although the configuration and operation of the receiving circuit in the fifth embodiment of the invention have been described on the basis of the receiving circuit in the first embodiment of the invention, the configuration and operation can be described in quite the same manner even if they are described on the basis of the receiving circuit in the second embodiment of the invention.

As is apparent from the above description, according to the present invention, the receiving circuit comprises means for generating a sum signal or a difference signal from signals of two paths received by the respective antennas, means for giving delay to either an output of the sum signal generating means or an output of the difference signal generating means, means for summationally combining an output of the delay means and the signal of the not-delayed path, a desired-wave pass filter means for receiving an output of the summationally combining means, a dividing means for receiving an output of the desired-wave pass filter means, an orthogonal detection means for receiving an output of the dividing means, and a filter means for receiving an output of the orthogonal detection means to extract a base band signal therefrom, wherein the receiving path including the summationally combining means and the following are made into one path. Accordingly, not only a space diversity function similar to that of the first conventional example having two receiving paths independently can be realized, but also the size and the power consumption can be reduced.

Claims

1. A receiving circuit, comprising:

a first antenna;
 a second antenna;
 means for generating a sum signal or a difference signal from signals of two paths received by said respective antennas;
 means for giving delay to either an output of said sum signal generating means or an output of said difference signal generating means;
 means for summationally combining an output of said delay means and the signal of the not-delayed path;
 desired-wave pass filter means for receiving an output of said summationally combining means;
 dividing means for receiving an output of said desired-wave pass filter means;
 orthogonal detection means for receiving an output of said dividing means; and
 filter means for receiving an output of said orthogonal detection means to extract a base band signal therefrom;
 wherein said receiving path includes said summationally combining means and the following are made into one path.

2. A receiving circuit according to Claim 1, wherein means for subtractively combining the output of said delay means and the signal of the not-delayed path is provided in place of said means for summationally combining the output of said delay means and the signal of the not-delayed path.

3. A receiving circuit according to Claim 1, further comprising intermediate-frequency converting means constituted by an intermediate-frequency local oscillation signal source, a frequency conversion mixer and an intermediate-frequency band filter is provided, wherein the output of said means for summationally combining the output of said delay means and the signal of the not-delayed path or the output of said means for subtractively combining the output of said delay means and the signal of the not-delayed path is applied to said intermediate-frequency converting means to thereby make the receiving path including the intermediate-frequency band stage and the following into one path.

4. A receiving circuit according to Claim 1, wherein individual frequency converting means are provided for the signals of said two paths obtained from said respective antennas, and said means for generating a sum signal and a difference signal from the signals of said two paths obtained by said respective frequency converting means are pro-

vided in an intermediate-frequency band to thereby make the receiving path including the intermediate-frequency band stage and the following into one path.

5. A receiving circuit according to Claim 1, wherein three or more antenna are provided to constitute three or more branches, and that means for generating a sum signal and a difference signal upon signals from the three or more paths, so that means for giving delay to all but one of outputs of said sum signal generating means or outputs of said difference signal generating means, means for summationally or subtractively combining an output of said delay means and the signal of the not-delayed path are provided to thereby make the receiving path including said combination means and the following into one path.

10

15

20

25

30

35

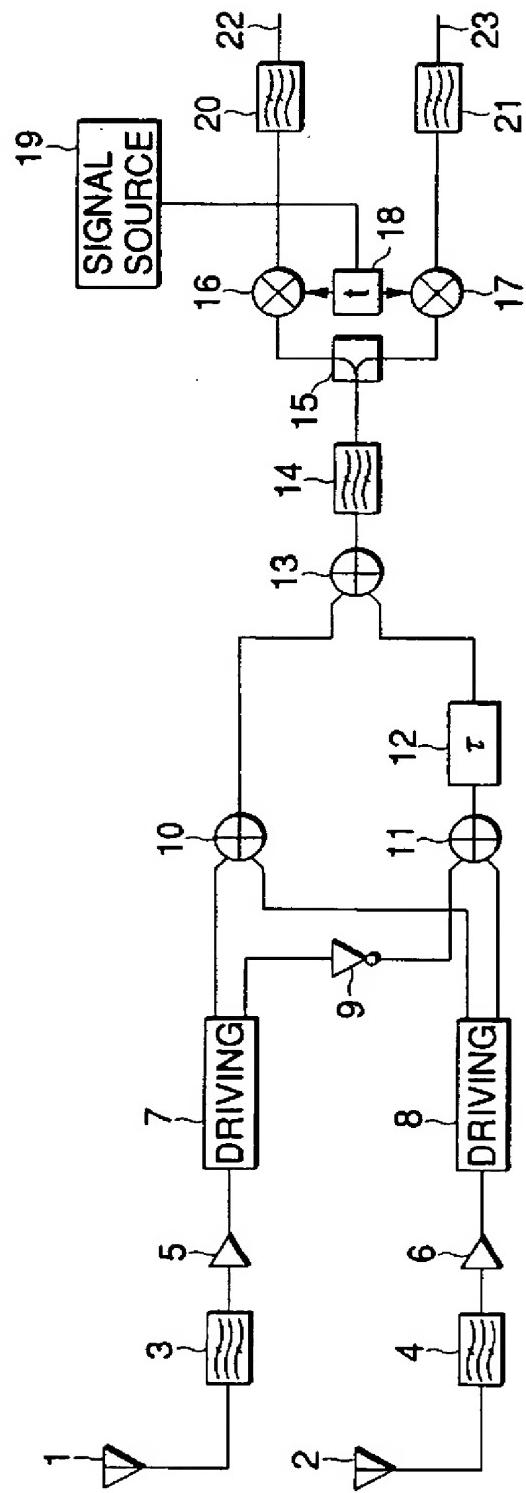
40

45

50

55

FIG.1



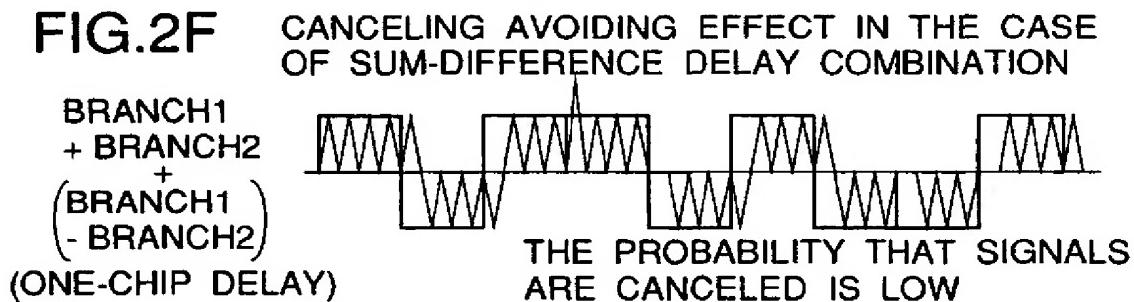
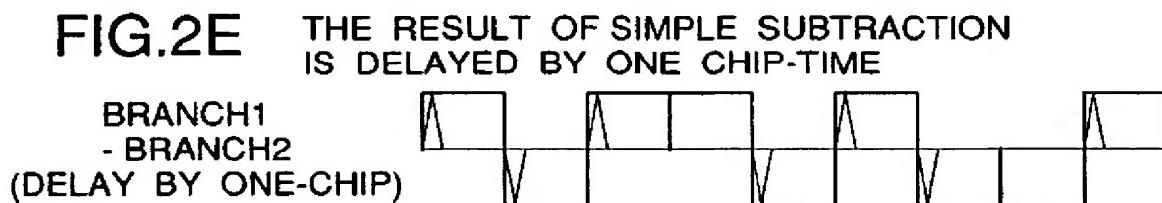
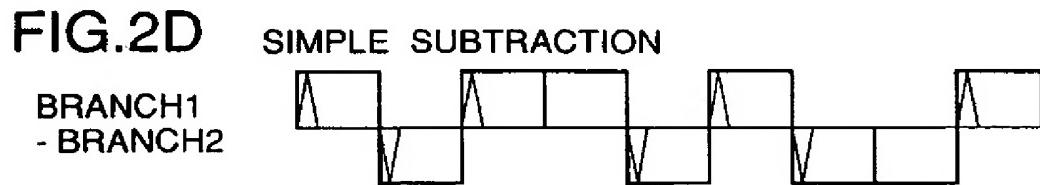
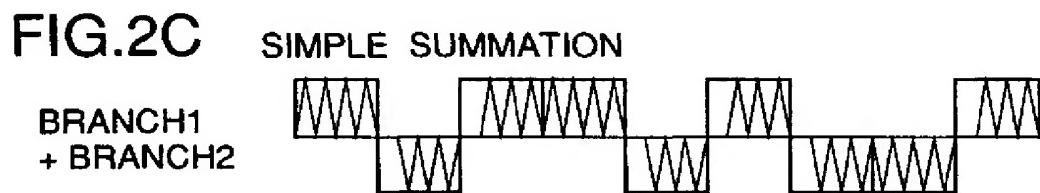
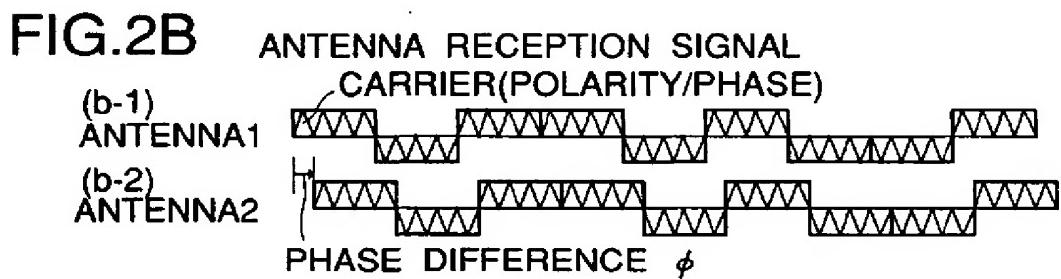
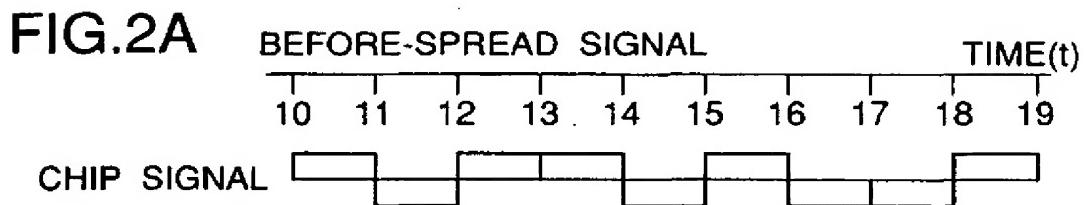


FIG.3A

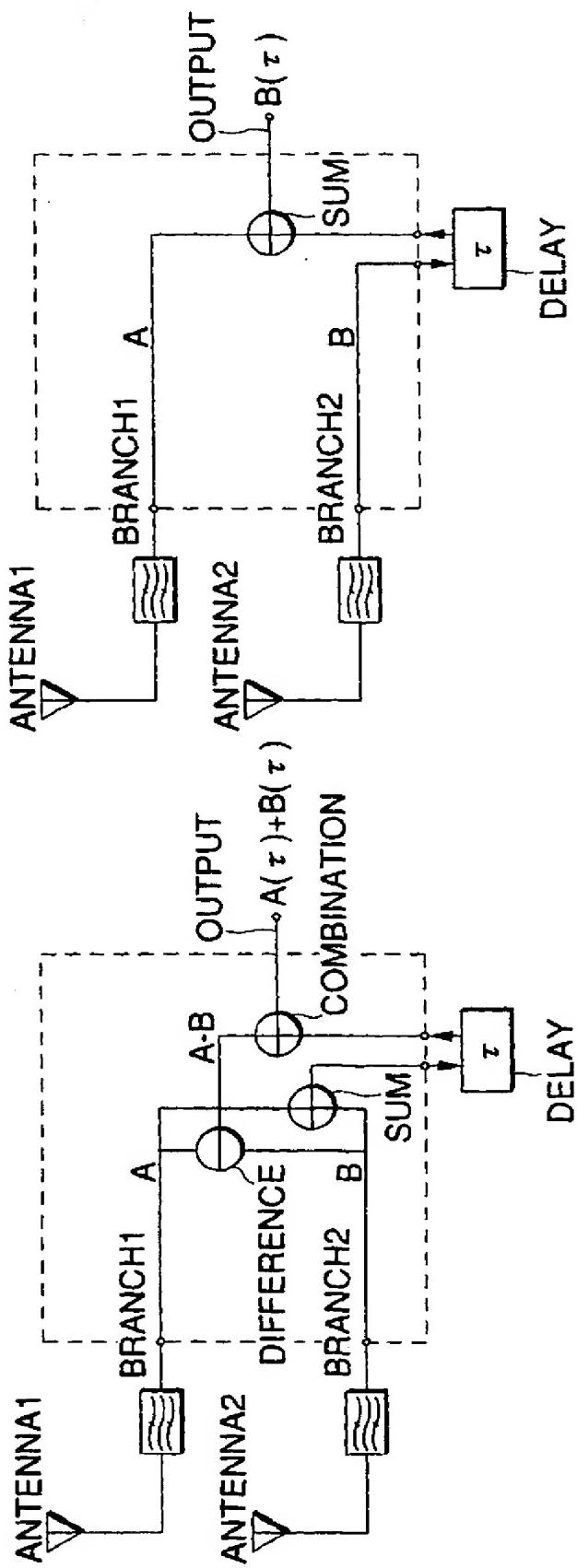


FIG.3B

FIG.4

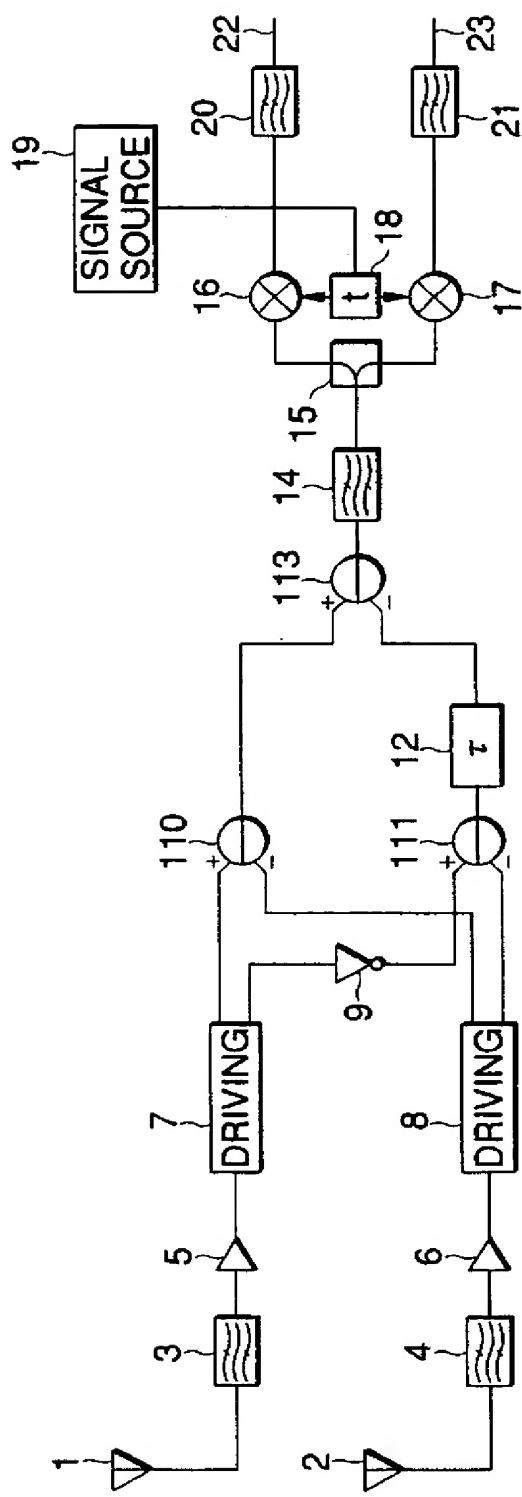


FIG.5

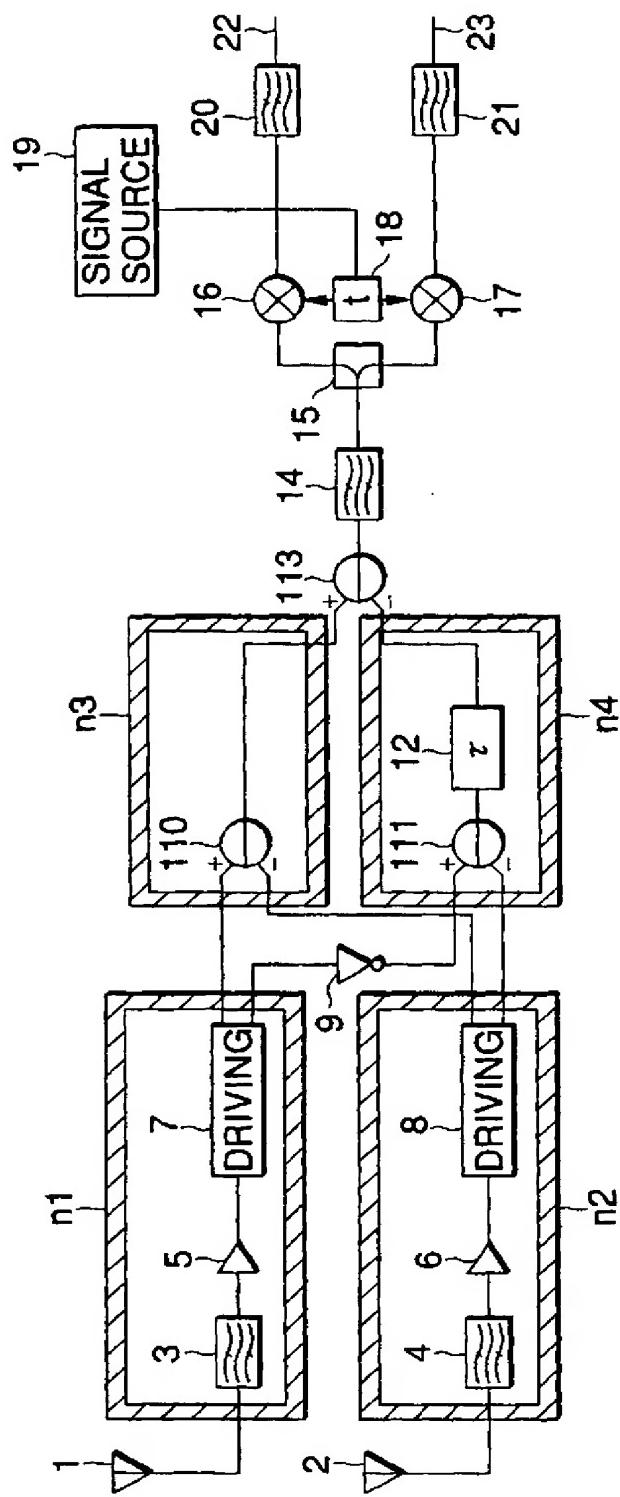


FIG.6

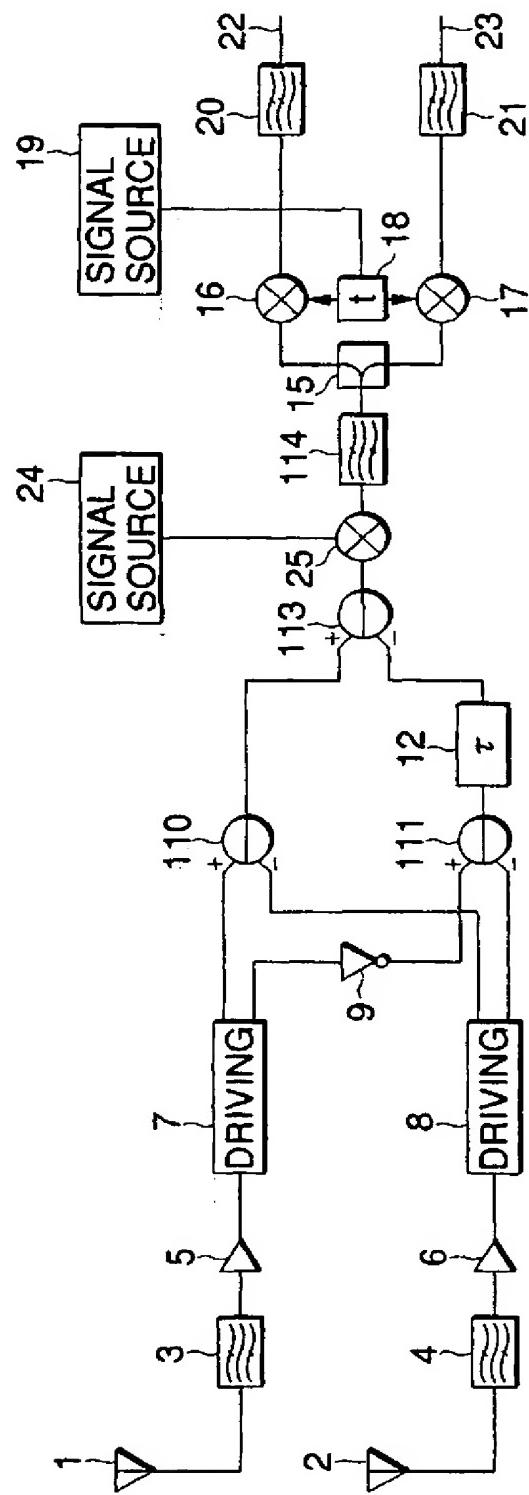


FIG.7

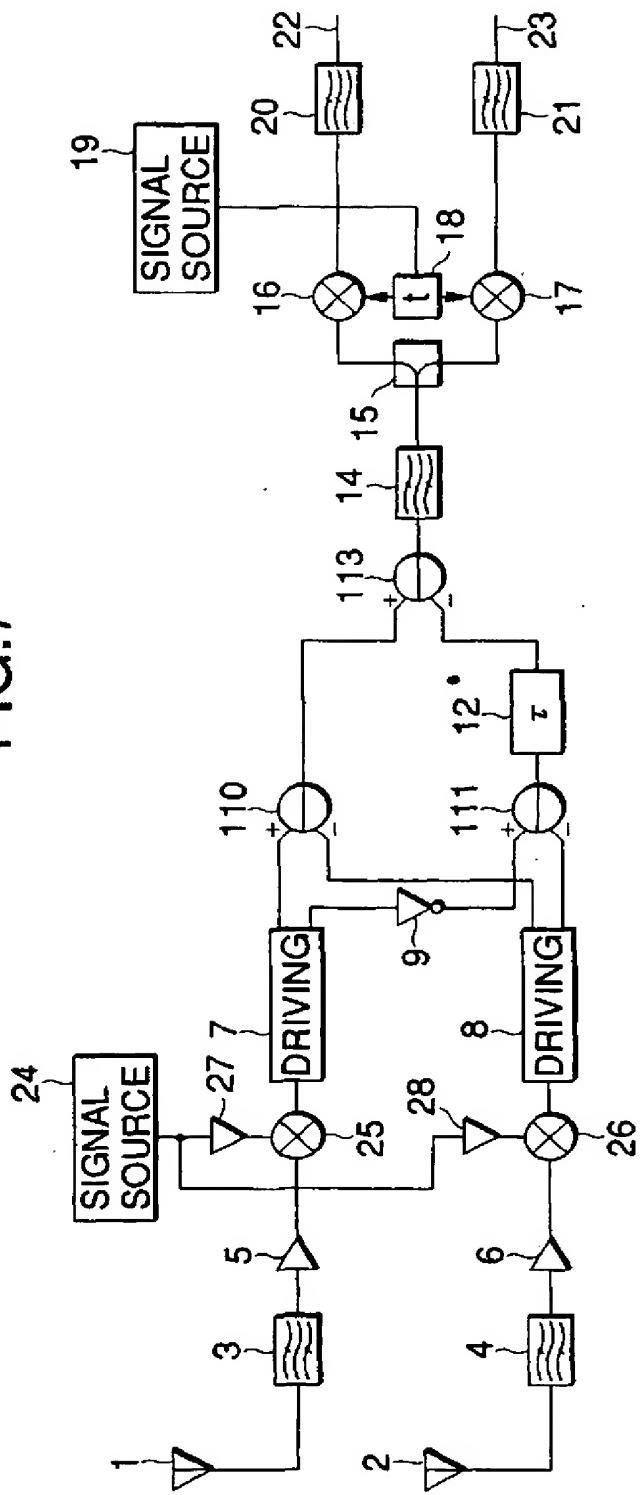


FIG.8

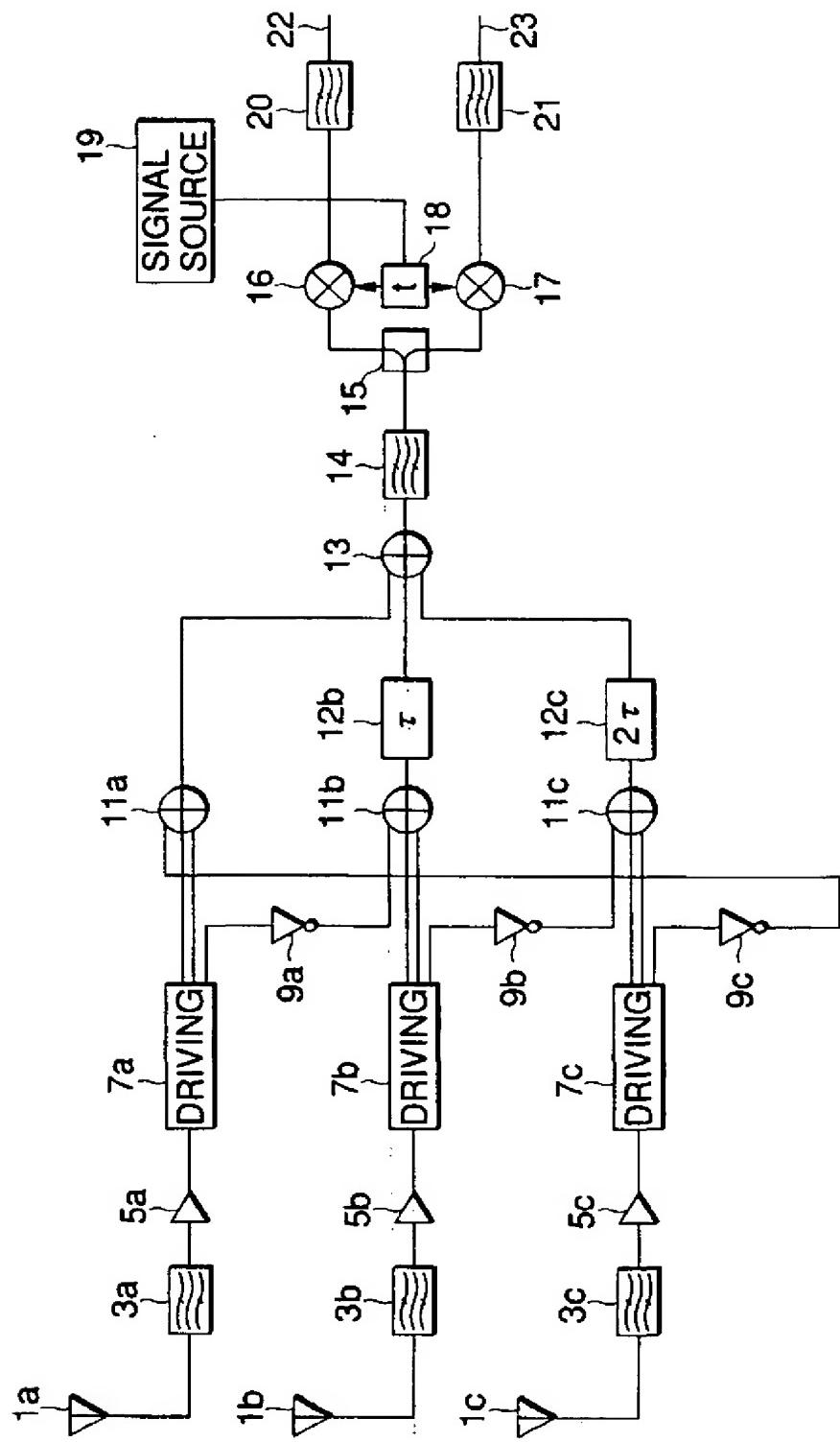


FIG.9

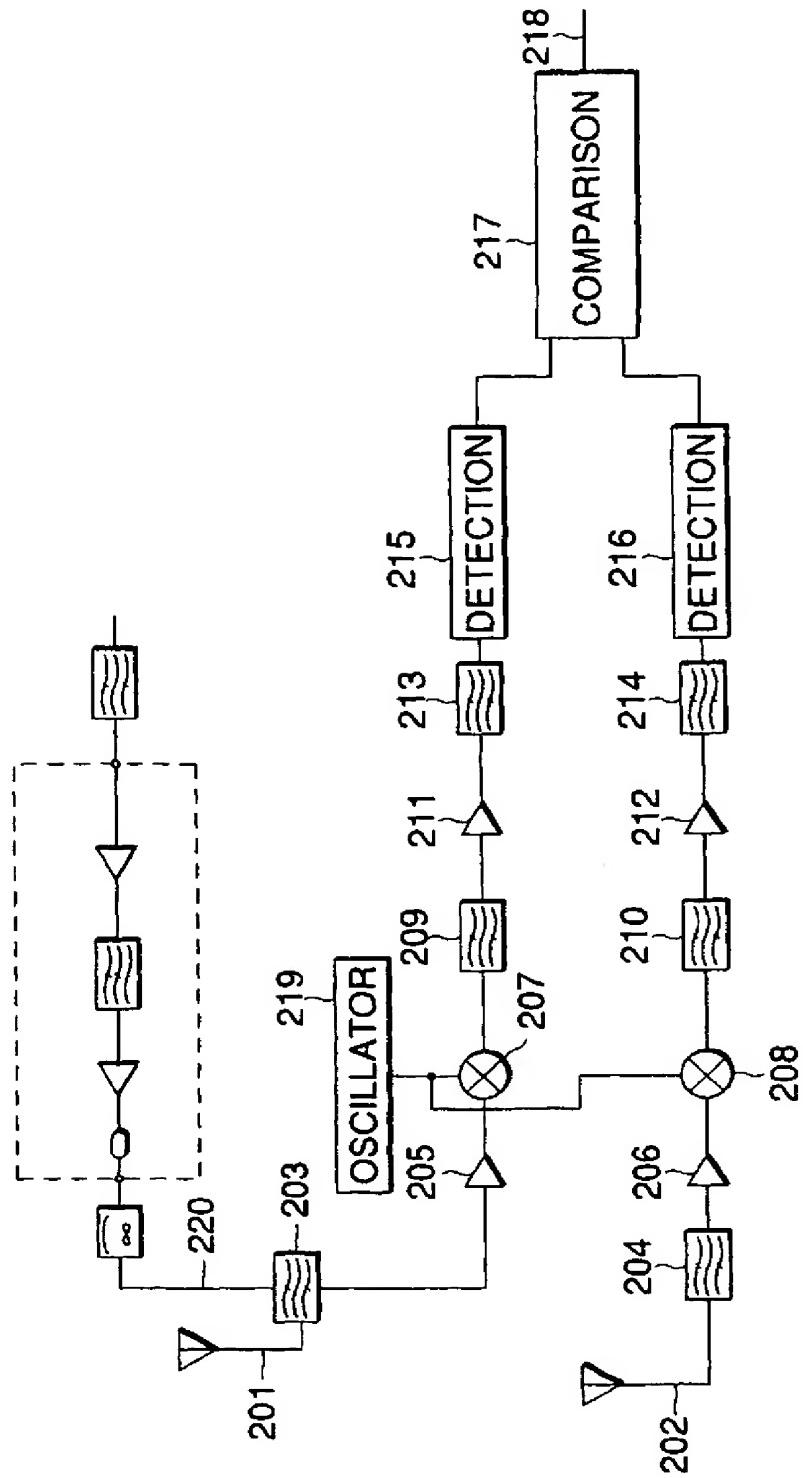
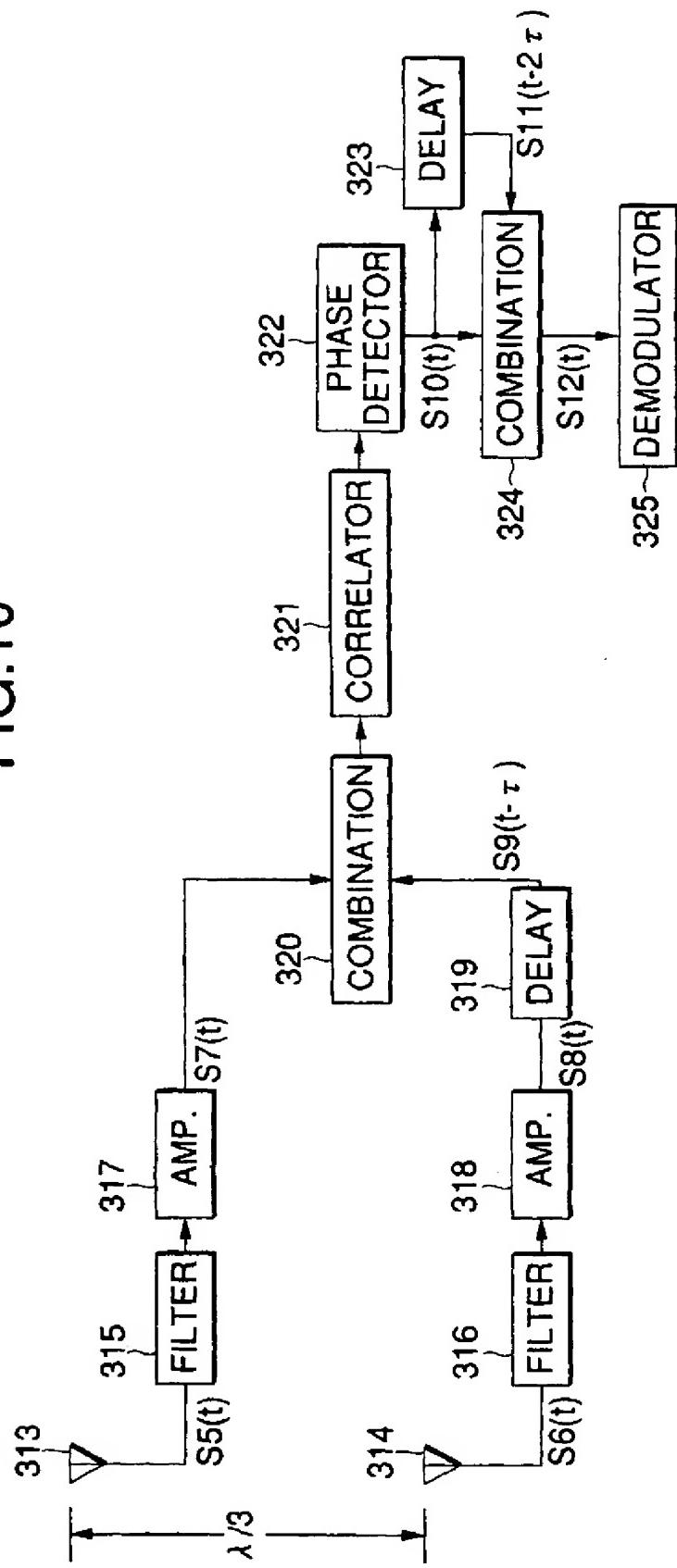
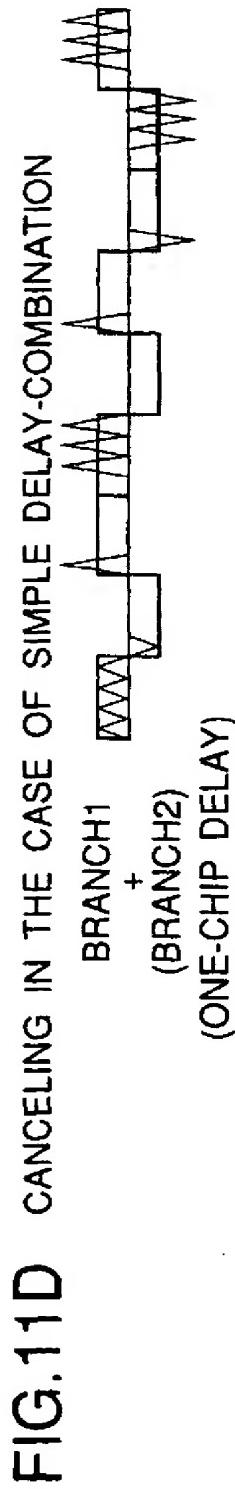
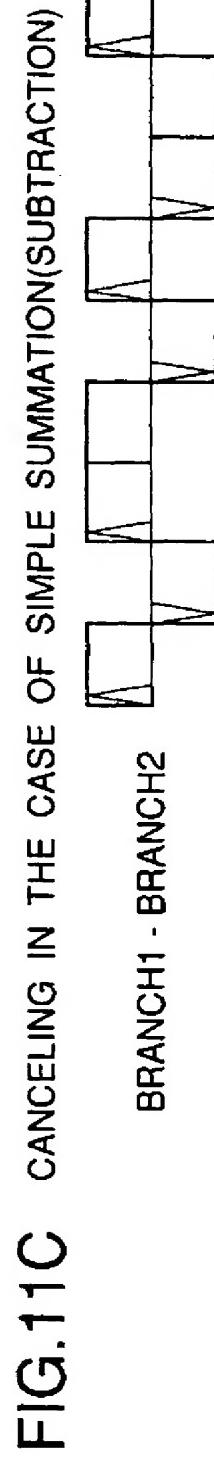
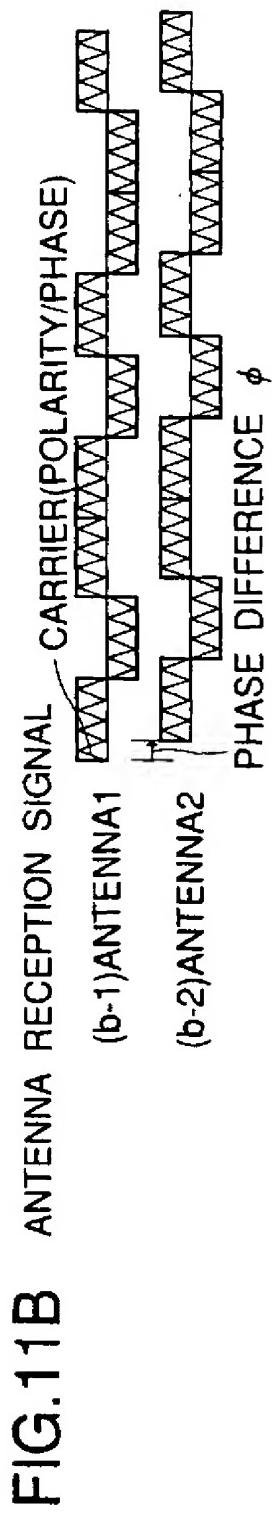
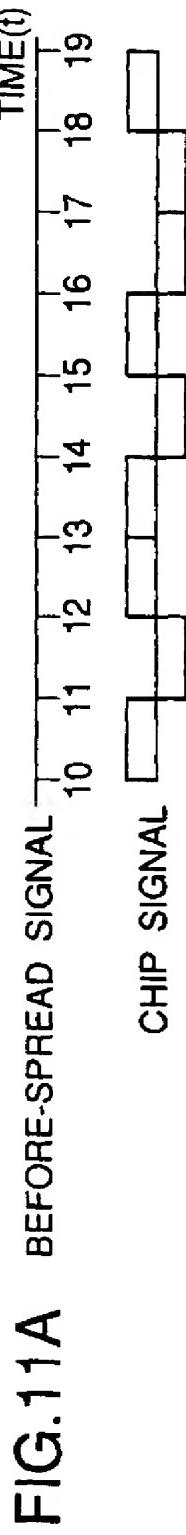


FIG.10





(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 851 605 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
02.04.2003 Bulletin 2003/14

(51) Int Cl.7: H04B 7/08, H04B 1/16

(43) Date of publication A2:
01.07.1998 Bulletin 1998/27

(21) Application number: 97122867.1

(22) Date of filing: 24.12.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC
NL PT SE

Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 27.12.1996 JP 35674896

(71) Applicant: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Kadoma-shi, Osaka-fu (JP)

(72) Inventors:

- Ohta, Gen-ichiro
Ebina-shi, Kanagawa (JP)

• Inogai, Kazunori
Yokohama-shi, Kanagawa (JP)
• Sasaki, Fujio
Yokohama-shi, Kanagawa (JP)
• Sudo, Hiraoki
Kanagawa, 224-0054 (JP)

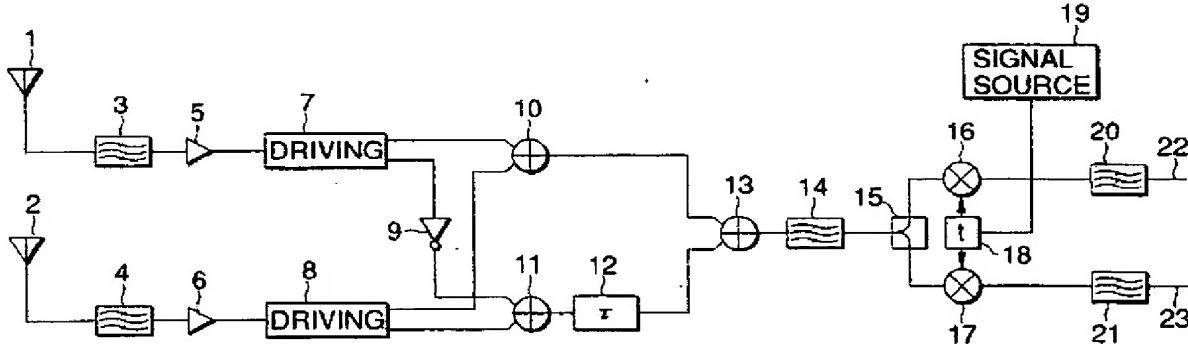
(74) Representative: Grünecker, Kinkeldey,
Stockmair & Schwahnhäuser Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Receiving circuit

(57) A receiving circuit includes a first antenna 1, a second antenna 2, units 10 and 11 for generating a sum signal or a difference signal from signals of two paths received by the respective antennas, a unit 12 for giving delay to either an output of the sum signal generating unit or an output of the difference signal generating unit, a unit 13 for summationally combining an output of the delay unit and the signal of the not-delayed path, a desired-wave pass filter unit 14 for receiving an output of

the summationally combining unit, a dividing unit 15 for receiving an output of the desired-wave pass filter unit, an orthogonal detection unit 16-19 for receiving an output of the dividing unit, and a filter unit 20 and 21 for receiving an output of the orthogonal detection unit to extract a base band signal therefrom, wherein the receiving path including the summationally combining unit and the following are made into one path to thereby attain miniaturization and low power consumption.

FIG.1



EP 0 851 605 A3



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 3 737 783 A (OSWALD J ET AL) 5 June 1973 (1973-06-05) * column 1, line 5 - line 18 * * column 1, line 52 - column 2, line 15 * * column 2, line 45 - column 3, line 25 * * column 3, line 35 - line 46; figure 1 * * column 4, line 41 - line 57; figure 2 * --- EP 0 582 233 A (NIPPON ELECTRIC CO) 9 February 1994 (1994-02-09) * page 3, line 17 - line 38; figure 2 * * page 3, line 54 - page 4, line 1; figure 3 * --- WO 96 31960 A (QUALCOMM INC) 10 October 1996 (1996-10-10) * page 18, line 19 - line 36; figure 3 * * page 27, line 17 - line 33; figure 8 * ----	1-5	H04B7/08 H04B1/16
A		1-5	
A		1-5	
TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04B			
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	10 February 2003	Sieben, S	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 97 12 2867

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

10-02-2003

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 3737783	A	05-06-1973	FR	2087370 A5	31-12-1971
			BE	766448 A1	29-10-1971
			DE	2123826 A1	23-12-1971
			GB	1327834 A	22-08-1973
			NL	7106635 A	17-11-1971
<hr/>					
EP 0582233	A	09-02-1994	JP	2982504 B2	22-11-1999
			JP	6053870 A	25-02-1994
			EP	0582233 A1	09-02-1994
			US	5425059 A	13-06-1995
<hr/>					
WO 9631960	A	10-10-1996	US	5608722 A	04-03-1997
			AU	698946 B2	12-11-1998
			AU	5529996 A	23-10-1996
			BR	9606291 A	02-09-1997
			CA	2191882 A1	10-10-1996
			CN	1149947 A ,B	14-05-1997
			EP	0763290 A1	19-03-1997
			FI	964820 A	03-02-1997
			JP	3043425 B2	22-05-2000
			JP	10501676 T	10-02-1998
			RU	2156033 C2	10-09-2000
			WO	9631960 A1	10-10-1996
<hr/>					

EPO/EPO/PAT/REGS

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82